A MULTIOCTAVE ACTIVE MMIC QUADRATURE PHASE SHIFTER

Patricia COGET*, Pascal PHILIPPE, Vlad PAUKER
Pierre DAUTRICHE, Patrick JEAN*

LEP : Laboratoires d'Electronique et de Physique appliquée
A member of the Philips Research Organization
3, avenue Descartes, 94450 LIMEIL-BREVANNES, France

ABSTRACT

This paper describes a 0.1 - 4.5 GHz GaAs monolithic quadrature phase shifter with very small phase error based upon a phase locked loop system. Such a wide band capability has been achieved by using FETs as voltage controlled resistors in a R-C all-pass phase shifter. This circuit, integrated in a broadband receiver produced an image rejection of at least 30 dB over the frequency band.

INTRODUCTION

Image frequency rejection in a wide band monolithic integrated receiver is not possible by prefiltering when the "IF/RF" ratio is low because of the low quality factor of inductive elements. Therefore an image frequency rejection mixer has to be used. It requires two 90° out of phase local oscillator signals.

In a very wide band (5 octaves) and relatively low frequency system (down to 0.1 GHz) a passive phase shifter cannot be used because of bandwidth limitations and excessive physical dimensions. Active solutions have been proposed that enable chip size to be reduced (1). However their relative bandwidth is still too limited, therefore, we have resorted to an active system where a phase lock loop automatically forces the LO signals into phase quadrature.

A similar system has been first proposed in a circuit operating at VHF frequencies (2). It consists (figure 1) of a voltage controlled phase shifter (P), a quadrature phase detector (C) and an integrator (I). The phase detector delivers a DC output signal when the LO signals departs from quadrature. This error signal is integrated and fed-back to the phase control input of the phase shifter. The system becomes stable when the integrator has zero input voltage, namely when quadrature is reached.

*TRT : Télécommunications Radioélectriques et Téléphoniques, 5 avenue Réaumur, 92350 LE PLESSIS ROBINSON, France

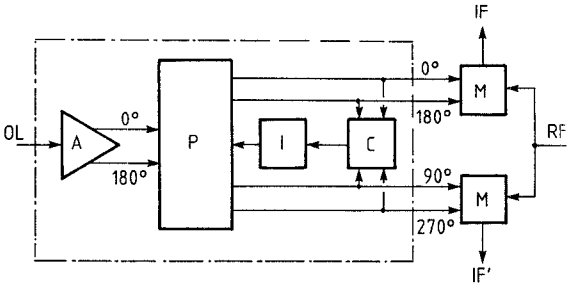

Figure 1 : Circuit diagram
All elements, except I, are integrated on the same chip)
A : input differential amplifier
P : voltage controlled phase shifter
C : phase comparator
I : integrator
M : double balanced mixer

CIRCUIT DESIGN

The phase shifter (figure 2) consists of two R-C all-pass networks with FETs used as voltage controlled resistors.

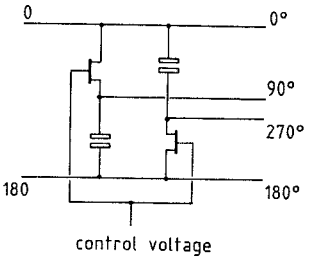

Figure 2 : Voltage controlled phase shifter

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It delivers four quadrature output signals as required for the operation of the double balanced mixers used in the receiver. The frequency range over which the quadrature can be obtained is limited by the dynamics of the channel resistance variation with gate voltage. The choice of the size of the capacitor and the transistor is given by a trade-off between two contradictory requirements :

- The R-C network must have a high impedance compared to the output impedance of the differential stage,
- But it must have a quite low impedance to minimize the amplitude mismatch between the 90°/270° and 0/180° outputs.

The input differential stage must deliver balanced signals with a precision better than 0.5°. In order to fullfil this requirement over the wide frequency range to be covered, three cascaded differential amplifiers have been used.

High linearity is required for the phase detector since distorsion can generate a parasitic DC output voltage. It consists of two double balanced ring mixers (figure 3) connected in parallel, with gate and drain input signals interchanged so that the four outputs of the phase shifter are loaded by identical impedances The phase detector has symmetrical DC outputs. This is necessary for the system to be unsensitive to an unwanted offset voltage (non zero DC output voltage when phase shift is 90°).

The integrator of course cannot be an ideal one. Although it has a very low cut-off frequency, it behaves as an amplifier with respect to DC voltage. This means that a systematic error exists in the system the magnitude of which will depend on the DC voltage gain of the integrator. Taking into account the slopes $d\varphi/dV$ and $dV/d\varphi$ of the phase shifter and the phase detector respectively, a DC voltage gain of a few thousand is necessary to ensure a phase error below 1°. This is achieved by using an external low cost operational amplifier.

Also of importance in the design is to minimize the low frequency noise in the RC all-pass network and the phase detector since it is converted into phase noise. This is the main reason for the use of unbiased FETs (Vds = 0),

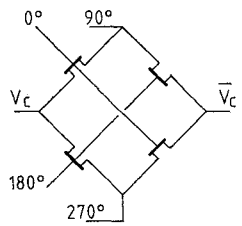

Figure 3 : Phase comparator circuit

which do not generate 1/f noise, in these parts of the circuit. The sensitivity to low frequency output noise of the detector is also strongly reduced by the loop integrator with very low cut-off frequency.

The circuit has been laid out as symmetrical as possible to make sure that signals have the desired phase shift. In particular, the length of signal paths between the input of the phase comparator and the input of mixers have been carefully equalized.

FABRICATION

The monolithic circuit (figure 4) containing the complete quadrature phase shifter (except the integrator) and two double balanced mixers has been processed at the Philips Microwave Foundry at Limeil-Brévannes, France. The circuit size is 1 x 2 mm^2 and contains 86 0.7 µm gate length FETs with widths ranging from 8 to 120 µm. In spite of the circuit complexity, the fabrication yield was 61 %.

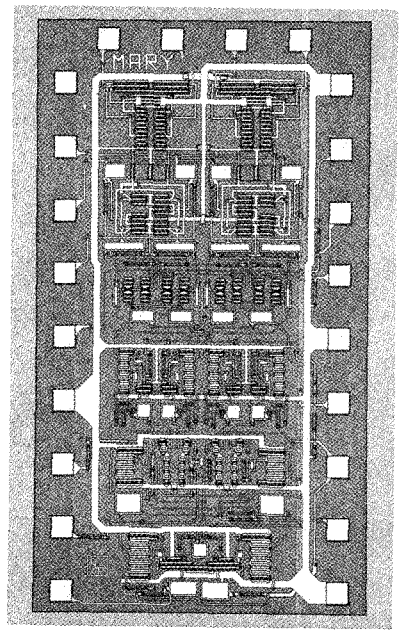

Figure 4 : photograph of the receiver

MEASUREMENTS

As the phase shifter was integrated in a broadband receiver, the direct measurement of the phase error and amplitude mismatch at the output of the phase shifter has not been possible. Therefore we have taken the image rejection level achieved by the receiver as indicator of the phase shifter performance although part of the phase error and amplitude mismatch can be due to the mixers. Image rejection is obtained by adding the IF and IF' output signals (figure 1) into a 0/90° combiner. The rejection is limited by the overall amplitude mismatch $\Delta A/A$ and phase error $\Delta\varphi$ introduced either by the system or by the external combiner according to :

$$R \# \frac{1}{2}\sqrt{\left(\frac{\Delta A_1}{A_1}+\frac{\Delta A_2}{A_2}\right)^2+\left(\Delta\varphi_1+\Delta\varphi_2\right)^2}$$

where the index 1 and 2 refer respectively to the system and the combiner. The figure 5 shows the rejection and the phase comparator output as a function of the phase shifter control voltage (open loop operation) at the optimum IF frequency for which the combiner errors are minima ($\Delta A_2/A_2 = 0, \Delta\varphi_2 = 0.5°$). The maximum rejection is obtained when the phase error of the combiner is compensated ($\Delta\varphi_1 + \Delta\varphi_2 = 0$). It is as high as 50 dB which means that the amplitude mismatch is about 0.05 dB between the mixer outputs. As expected, simultaneously to maximum rejection a nearly zero DC differential voltage is observed at the output of the phase comparator.

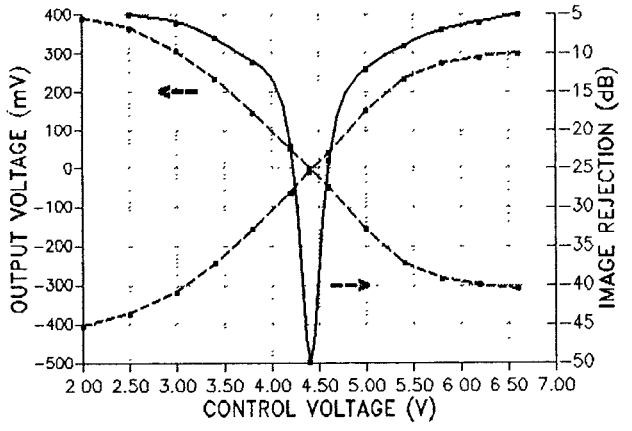

Figure 5 :
Phase detector output voltage and image frequency rejection (open loop operation)

In quadrature phase locked operation, the rejection level varies between 50 and 30 dB over the 0.1 - 4.5 GHz frequency band (figure 6).

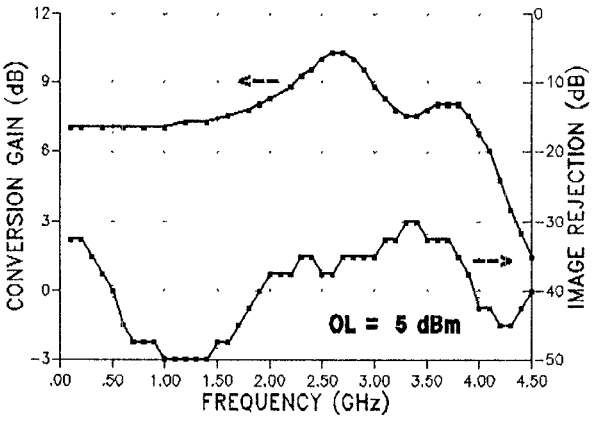

Figure 6 :
Image frequency rejection in closed loop operation

The decrease in the rejection level at high frequencies is mainly due to the amplitude mismatch that reaches 0.5 dB, probably because of a slight difference in the conversion gain between the two mixers. The overall phase error is quite low since to a rejection level of 30 dB with 0.5 dB of mismatch corresponds a phase error of less than 2°.

The conversion gain of the receiver (figure 6) is about 8-10 dB up to 4 GHz. Strong decrease is observed above because of simultaneous cut-off of mixer and phase shifter.

CONCLUSION

An active phase locked loop quadrature phase shifter which can operate over a very wide band (0.1 - 4.5 GHz) has been demonstrated for the first time. The main feature of this system is that it has a very small phase error, which is a major improvement compared to passive or even active phase shifter already reported. This phase shifter has been used within a broadband receiver which has achieved an image rejection of at least 30 dB over the 0.1 - 4.5 GHz frequency band.

REFERENCES

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